What Is Claimed Is:

1. An array substrate for a liquid crystal display device, comprising:

a substrate;

a plurality of gate lines arranged transversely on the substrate;

a plurality of data lines disposed orthogonal to the plurality of gate lines;

a plurality of thin film transistors formed on the substrate adjacent to intersections of the gate lines and the data lines, each thin film transistor including a gate electrode, a gate insulation layer, an active layer, an ohmic contact layer, a source electrode, and a drain electrode;

a plurality of pixel electrodes disposed at pixel regions defined by the intersections of the gate lines and the data lines, each pixel electrode connected to a corresponding one of the drain electrodes; and

a metal layer formed on an entire surface of each of the data lines.

2. The array substrate according to claim 1, wherein the gate insulation layer is disposed on the gate electrode.

3. The array substrate according to claim 1, wherein the active layer is disposed on the gate insulation layer, and the ohmic contact layer is disposed on the active layer.

4. The array substrate according to claim 1, wherein the source electrode and the drain electrode are disposed on the ohmic contact layer.

5. The array substrate according to claim 4, wherein the source electrode extends from one of the data lines.

6. The array substrate according to claim 4, wherein the drain electrode extends from one of the pixel electrodes.

7. The array substrate according to claim 4, wherein the drain electrode and source electrode include at least a transparent conductive material.

8. The array substrate according to claim 7, wherein each data line includes at least the transparent conductive material.

9. The array substrate according to claim 7, wherein each pixel electrode includes the transparent conductive material.

10. The array substrate according to claim 7, wherein the transparent conductive material is selected from a group including indium tin oxide, indium zinc oxide, zinc oxide, thin oxide and indium oxide.

11. The array substrate according to claim 1, wherein the gate insulation layer is disposed on the plurality of gate lines.

12. The array substrate according to claim 1, wherein the metal layer is selected from a group including aluminum (Al), copper (Cu), gold (Au) and silver (Ag).

13. The array substrate according to claim 12, wherein the metal layer is formed on an entire surface of the source electrode.

14. The array substrate according to claim 12, wherein the metal layer is formed at peripheral portions of the plurality of pixel electrodes.

15. The array substrate according to claim 12, wherein the metal layer is formed at peripheral portions of the drain electrode.

16. A method of fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a first metal layer on a substrate;

forming a gate line and a gate electrode;

forming a gate insulation layer to cover the first metal layer;

forming a pure amorphous silicon layer and a doped amorphous silicon layer on the gate insulation layer;

forming an ohmic contact layer and an active layer over the gate electrode;

forming a transparent conductive material on the gate insulation layer to cover the active layer and the ohmic contact layer;

forming a photoresist layer on the transparent conductive material;

patterning the photoresist layer using a mask;

forming a data line, a pixel electrode, a source electrode and a drain electrode; and

forming a second metal layer on an entire surface of the data line.

17. The method according to claim 16, wherein the step of forming the gate line and the gate electrode includes patterning the first metal layer.

18. The method according to claim 16, wherein the step of forming the ohmic contact layer and the active layer includes patterning the doped amorphous silicon layer and the pure amorphous silicon layer.

19. The method according to claim 16, wherein the mask includes a plurality of slits and a plurality of light shielding areas.

20. The method according to claim 16, wherein the step of forming the data line, the pixel electrode, the source electrode, and the drain electrode includes patterning the transparent conductive material using a dry etching process.

21. The method according to claim 20, wherein the step of patterning the transparent conductive material includes removing a first photoresist layer formed on the data line and the source electrode while etching exposed portions of the transparent conductive material, and removing peripheral portions of a second photoresist layer formed on the drain electrode and the pixel electrode while etching the exposed portions of the transparent conductive material.

22. The method according to claim 16, further including the step of forming the second metal layer on an entire surface of the source electrode.

23. The method according to claim 16, further including the step of forming the second metal layer at peripheral portions of the pixel electrode and the drain electrode.

24. The method according to claim 16, wherein the step of patterning the photoresist layer includes aligning the mask over the photoresist layer, exposing light through a plurality of slits of the mask; and developing the photoresist layer to expose the transparent conductive material.

25. The method according to claim 16, wherein the step of forming the second metal layer includes electroplating a second metal material on the data line, electroplating the second metal material on the source electrode, electroplating the second metal material on peripheral portions of the pixel electrode, electroplating the second metal material on peripheral portions of the drain electrode, and removing the photoresist layer from the transparent conductive material.

26. The method according to claim 16, wherein the source electrode extends from one of the data lines.

27. The method according to claim 16, wherein the drain electrode extends from one of the pixel electrodes.

28. The method according to claim 16, wherein the transparent conductive material is selected from a group including indium tin oxide, indium zinc oxide, zinc oxide, thin oxide and indium oxide.

29. The method according to claim 16, wherein the second metal layer is selected from a group including aluminum(Al), copper(Cu), gold (Au) and silver (Ag).